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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
1400.4100220	

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on 10-27-2006

Signature /Ross D. Snyder/

Typed or printed name Ross D. Snyder, Reg No 37730

Application Number	Filed
09/746,602	12-21-2000

First Named Inventor: James S. McCormick et al.

Art Unit	Examiner
2616	Hsu, Alpus

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 37,730
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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Signature

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Typed or printed name

512-347-9223
Telephone number

10-27-2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): James S. McCormick, et al.

Title: MULTIPROCESSOR CONTROL BLOCK FOR USE IN A COMMUNICATION SWITCH AND METHOD THEREFORE

App. No.: 09/746,602 Filed: 12-21-2000

Examiner: Hsu, Alpus Group Art Unit: 2616

Atty. Dkt. No. 1400.4100220

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Claims 1-31 are pending in the present application. The Examiner has allowed claims 1-23. The Examiner has rejected claims 24-29. The Examiner has objected to claims 30 and 31. Appellant respectfully requests reconsideration of pending claims 24-31. Appellant files herewith a notice of appeal. Pursuant to the "New Pre-Appeal Brief Conference Pilot Program," 1296 Off. Gaz. Pat. Office 67 (July 12, 2005) and the "Extension of the Pilot Pre-Appeal Brief Conference Program" dated 1/10/2006, Appellant submits a pre-appeal brief request for review. The review is requested for the reasons set forth below:

Appellant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection. Appellant submits the Examiner's "Response to Arguments" provides evidence that the Examiner has failed to consider the pending claims as required by the Manual of Patent Examining Procedure (MPEP) and prevailing case law. For anticipation under 35 U.S.C. § 102, a reference must teach every aspect of the claimed invention either explicitly or implicitly. Any feature not directly taught must be inherently present [emphasis added]. See MPEP 706.02 – distinction between 35 U.S.C. § 102 and § 103. As Appellant describes in detail below, Appellant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection.

The Examiner has rejected claims 24, 28, and 29 under 35 U.S.C. § 102(b) as being anticipated by Kobayashi in U.S. Patent No. 4,775,974. Appellant respectfully disagrees.

Regarding claim 24, Appellant submits the cited reference fails to disclose the features of claim 24. For example, Appellant submits the cited portions of the cited reference fail to disclose a method for processing ingress data units in a link layer processor of a multiprocessor control block in a communication switch, comprising: receiving a first ingress data unit corresponding to a call; selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block; and forwarding the first ingress data unit to the first selected intermediate processor. Appellant notes col. 3, lines 22-26, of Kobayashi states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." Appellant submits link layer processor 21 does not appear to perform the steps of selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block or forwarding the first ingress data unit to the first selected intermediate processor. Moreover, Appellant notes the quote above from Kobayashi recites "outgoing frames," not "a first ingress data unit." Thus, Appellant submits the cited portions of the cited reference fail to disclose the subject matter of claim 24. Therefore, Appellant submits claim 24 is in condition for allowance.

Regarding claims 28 and 29, Appellant submits the cited reference fails to disclose the features of claims 28 and 29. For example, Appellant submits the cited portion of the cited reference fails to disclose assigning a sequence number to the first ingress data unit, wherein the sequence number corresponds to the call. Rather, the Examiner cites different features of different elements of the cited reference. The Examiner cites col. 4, lines 29-33 and 39-42, which relate, respectively, to an error detector 61 of link layer processor 21 and a frame sequence number generator 65 of link layer processor 21 but then cites col. 5, lines 34-39, which relate to a header updating circuit 76 of packet layer processor 24. Appellant submits, based on the teachings of the cited portions of the cited reference, the functionality of the error detector 61 and/or frame sequence number generator 65 of link layer processor 21 cannot be imputed to header updating circuit 76 of packet layer processor 24, nor can the functionality of the header updating circuit 76 of packet layer processor 24 be imputed to error detector 61 and/or frame sequence number generator 65 of link layer processor 21. In paragraph 9 of the final Office action, the Examiner states, "...it is well known in the art and commonly applied in data communications field for assigning a sequence number to data packet for data

assembly/disassembly and error detection/correction purposes." However, Appellant notes the Examiner has failed to cite any reference in support of such assertion. Moreover, Appellant submits the Examiner's assertion fails to address the feature "...wherein the sequence number corresponds to the call" found in claim 28. Thus, Appellant submits the Examiner has failed to make a *prima facie* showing of anticipation. Therefore, Appellant submits claims 28 and 29 are in condition for allowance.

As another example, with respect to claim 29, Appellant submits the cited portions of the cited reference fail to disclose receiving a second ingress data unit corresponding to the call; assigning the sequence number corresponding to the call to the second ingress data unit; selecting a second selected intermediate processor of the plurality of intermediate processors; and forwarding the second ingress data unit to the second selected intermediate processor. Appellant again notes col. 3, lines 22-26, of Kobayashi, which states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." Accordingly, Appellant submits the cited portion of the cited reference appears to fail to teach receiving a second ingress data unit corresponding to the call;...and forwarding the second ingress data unit to the second selected intermediate processor. Moreover, Appellant submits the Examiner's assertion fails to address the feature "...assigning the sequence number corresponding to the call to the second ingress data unit..." found in claim 29. Thus, Appellant submits the Examiner has failed to make a *prima facie* showing of anticipation. Thus, Appellant submits claim 29 is in condition for allowance.

The Examiner has rejected claims 25-27 under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi in U.S. Patent No. 4, 775,974 in view of Tzeng in U.S. Patent No. 6,438,135. Appellant respectfully disagrees.

Regarding claim 25, the Examiner acknowledges, "KOBAYASHI differs from the claim, in that, it fails to disclose the selection of the first selected intermediate processor based on a prioritization scheme...." Appellant submits both the Kobayashi and Tzeng references, either alone or in combination, fail to anticipate or render obvious the features of claim 25. For example, Appellant submits the Kobayashi reference teaches away from the aspects of teachings of Tzeng alleged by the Examiner. Appellant again notes col. 3, lines 22-26, of Kobayashi, which states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." As Appellant submits

Kobayasi expressly teaches the outgoing frames (not ingress data units) are "individually separated according to their destinations," Appellant submits Kobayashi teaches away from wherein selecting the first selected intermediate processor further comprises selecting the first selected intermediate processor based on a prioritization scheme. Moreover, as Appellant has noted, Appellant submits link layer processor 21 does not appear to perform the steps of selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block. Thus, Appellant submits the cited portions of the cited references, either alone or in combination, fail to anticipate or render obvious the features of claim 25. Therefore, Appellant submits claim 25 is in condition for allowance.

Regarding claims 26 and 27, the Examiner acknowledges, "Kobayashi differs from the claim, in that, it fails to disclose the prioritization scheme includes a round robin scheme and at least partially based on loading on each intermediate processor of the plurality of intermediate processors...." Appellant submits both the Kobayashi and Tzeng references, either alone or in combination, fail to anticipate or render obvious the features of claims 26 and 27. For example, Appellant submits the Kobayashi reference teaches away from the aspects of teachings of Tzeng alleged by the Examiner. Appellant again notes col. 3, lines 22-26, of Kobayashi, which states, "Link layer processor 21 is connected to demultiplexer 23 where outgoing frames are individually separated according to their destinations for coupling to packet layer processors 24-1 to 24-n." As Appellant submits Kobayasi expressly teaches the outgoing frames (not ingress data units) are "individually separated according to their destinations," Appellant submits Kobayashi teaches away from wherein selecting the first selected intermediate processor further comprises selecting the first selected intermediate processor based on a prioritization scheme and further teaches away from wherein the prioritization scheme includes a round robin scheme or wherein the prioritization scheme is at least partially based on loading on each intermediate processor of the plurality of intermediate processors. Moreover, as Appellant has noted, Appellant submits link layer processor 21 does not appear to perform the steps of selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block. Thus, Appellant submits the cited portions of the cited references, either alone or in combination, fail to anticipate or render obvious the features of claims 26 and 27. Therefore, Appellant submits claims 26 and 27 are in condition for allowance.

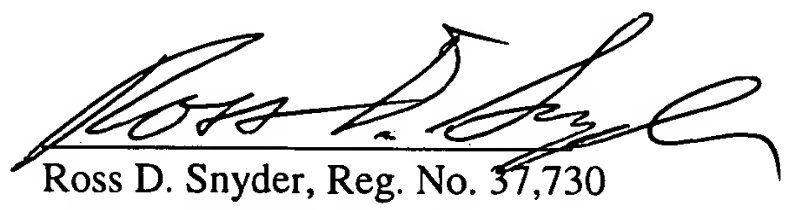
As another example, with respect to claim 27, Appellant notes can find no teaching in col. 4, lines 49-57 of the Tzeng reference, as cited by the Examiner, of wherein the prioritization scheme is at

least partially based on loading on each intermediate processor of the plurality of intermediate processors. Thus, even if an attempt were made to combine the teachings of the cited portions of the cited references, Appellant submits such attempt would not yield the features recited in claim 27. Moreover, Applicant submits the Examiner appears to be alleging "...the service weight of the priority queue 20" (col. 4, lines 49-57 of Tzeng, as cited by the Examiner) teaches or renders obvious "...wherein the prioritization scheme is at least partially based on loading on each intermediate processor of the plurality of intermediate processors." However, Applicant notes Tzeng states, in col. 4, lines 12-15, "The value of the service weight for each priority queue 20 is predetermined by either a default setting or by a network administrator." Applicant submits such teaching fails to anticipate or render unpatentable the subject matter of claim 27. Thus, Appellant submits claim 27 remains nonobvious over the cited portions of the cited references, either alone or in attempted combination. Therefore, Appellant submits claim 27 is in condition for allowance.

The Examiner has allowed claims 1-23. The Examiner has objected to claims 30 and 31 but states they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Appellant has presented arguments for the allowability of at least one claim from which claims 30 and 31 depend. Thus, Appellant submits claims 30 and 31 are also in condition for allowance.

Respectfully submitted,

10/27/2006
Date



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